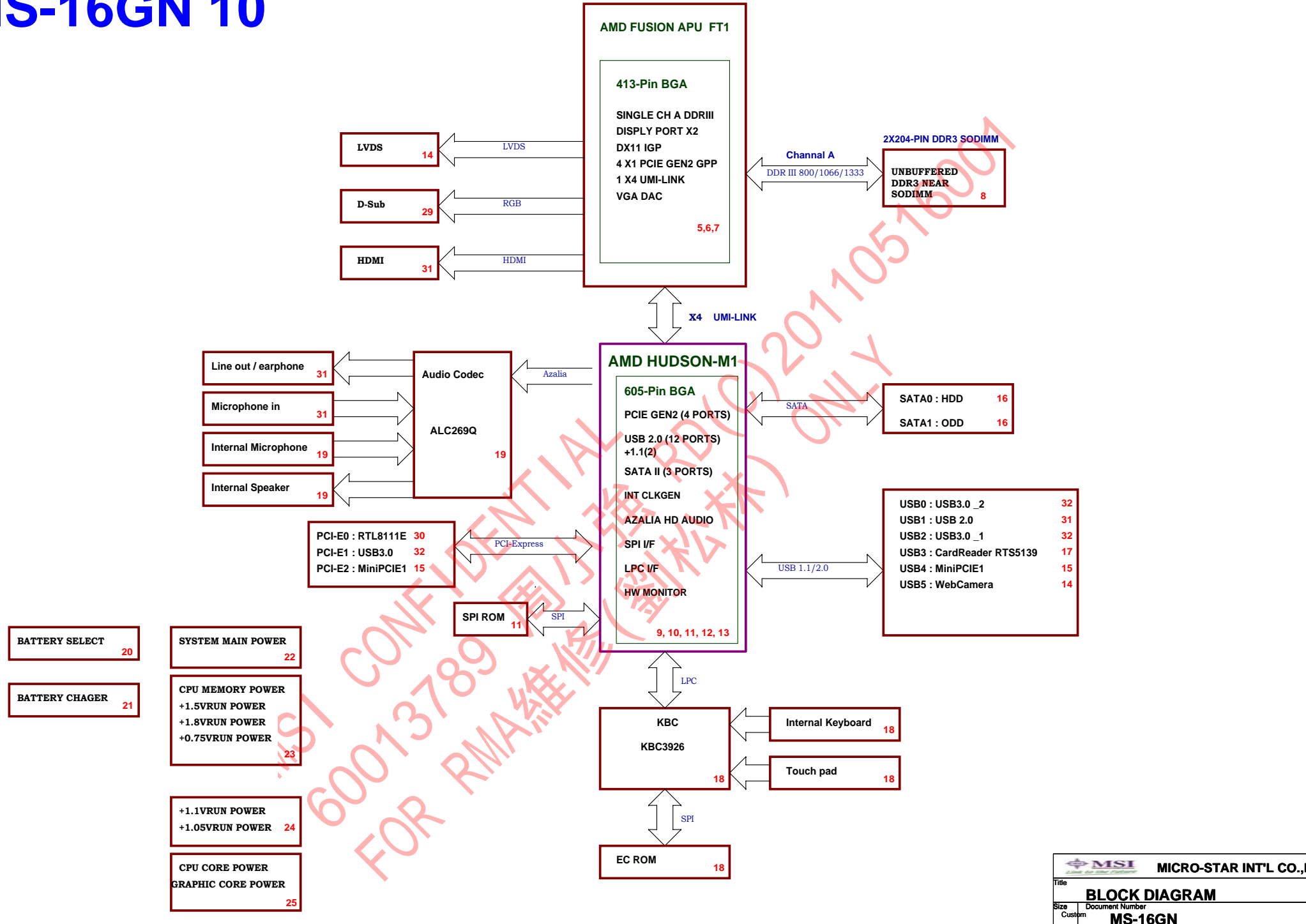
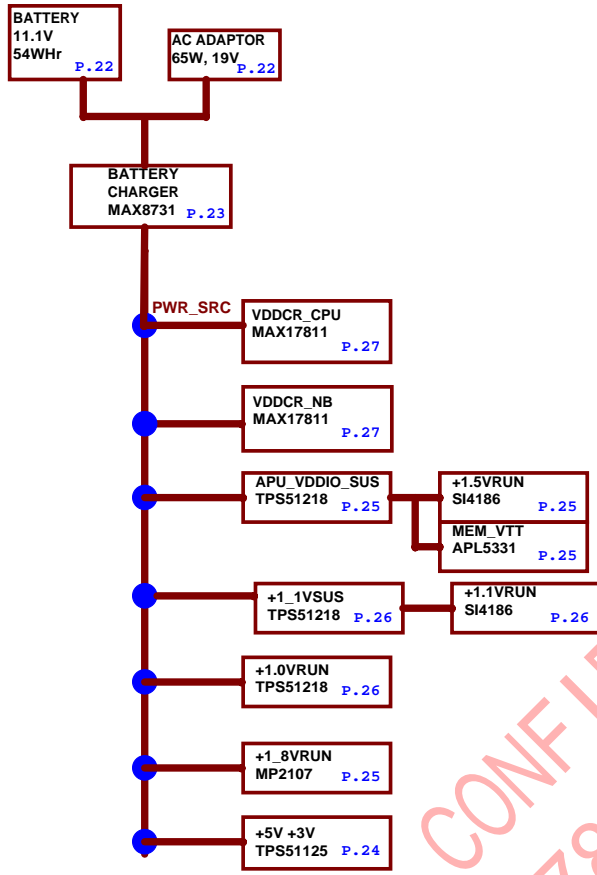


MS-16GN 10

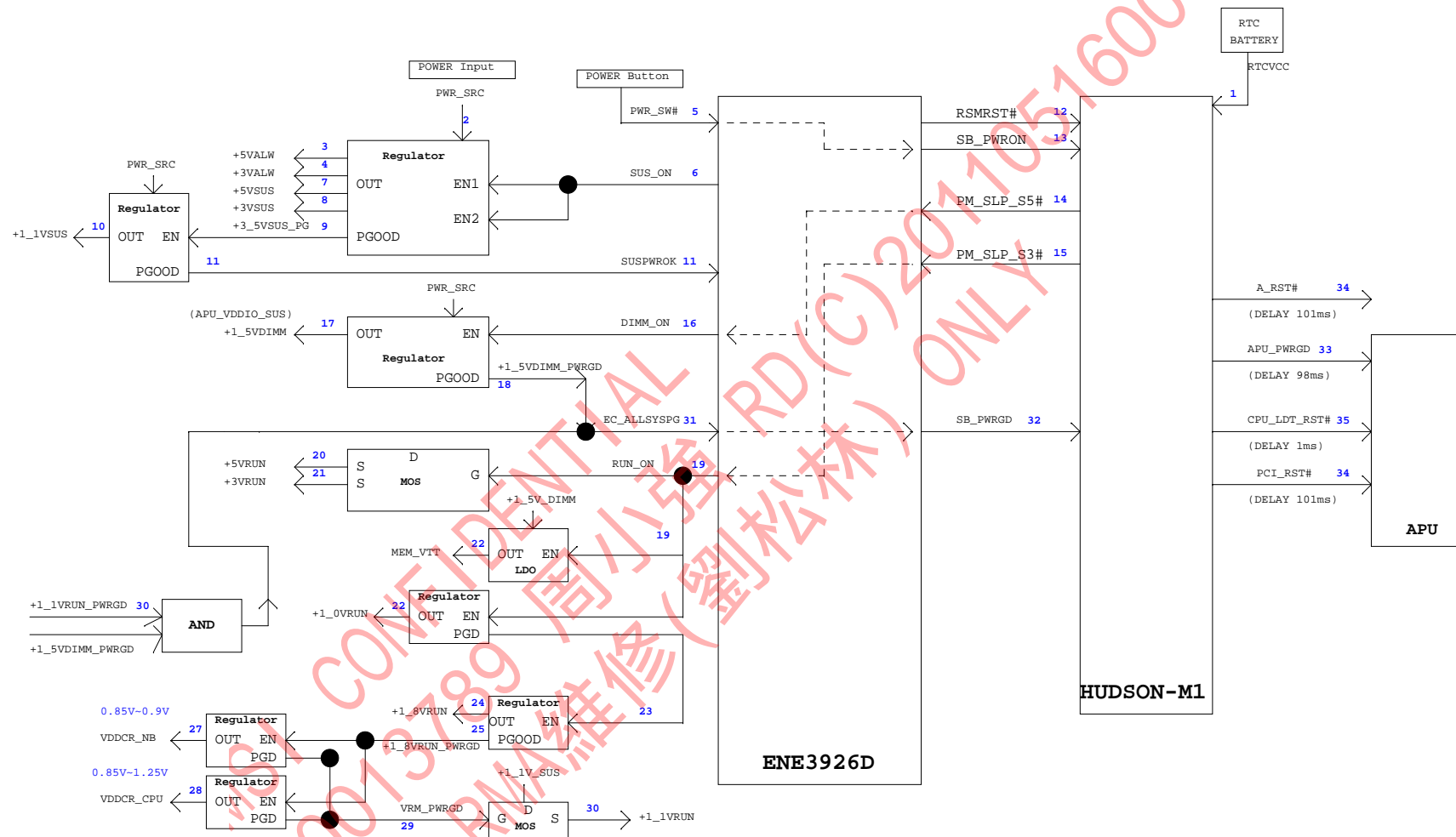




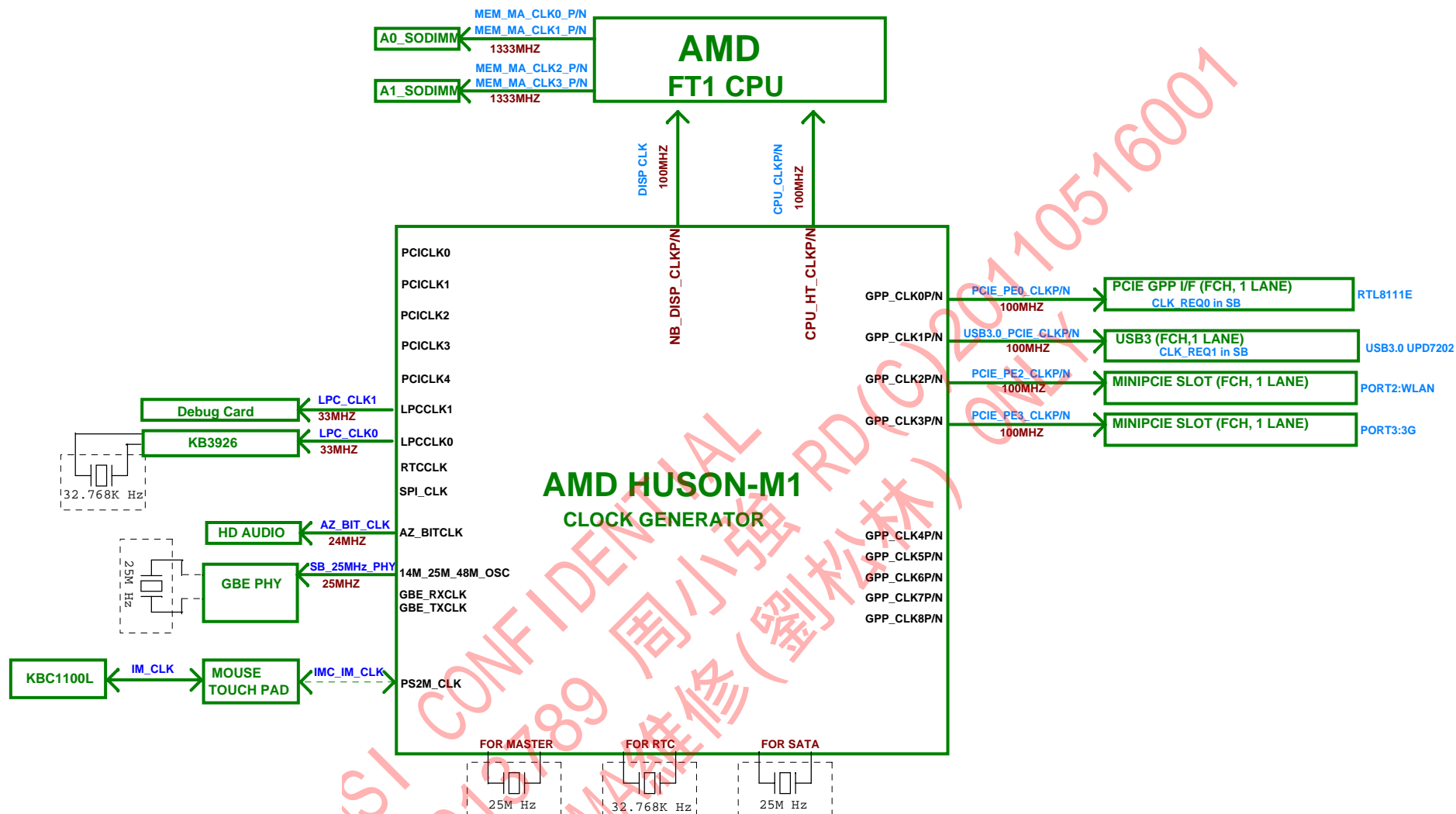
AMD FT1	
VDDCR_CPU	VDDCR_CPU 0.85V--1.25V 11A
VDDCR_NB	VDDCR_NB 0..85V~0.9V 10A
APU_VDDIO_SUS	APU_VDDIO_SUS 2A
+1.8VRUN	VDD18 2A ;VDD_18_DAC 0.15A
+1.0VRUN	VDD_10 5.5A;VDDPL_10 0.2A
+3VRUN	VDD33 0.5A

HUDSON-M1	
+3VRUN	VDDIO_33_PCIGP 3.3V 0.042A
+1_8VRUN	VDDIO_18_FC 1.8V 0.050A
+1.1VRUN	VDDAN_11_PCIE 1.1V 1.115A
+3VRUN	VDDPL_33_PCIE 3.3V 0.022A
+1.1VRUN	VDDAN_11_SATA 1.1V 1.3A
+3VRUN	VDDPL_33_SATA 3.3V 0.015A
+3VSUS	VDDAN_33_USB_S 3.3V 0.53A
+1_1VSUS	VDDAN_11_USB_S 1.1V 0.09A
+1.1VRUN	VDDCR_11_1V 0.79A
+1.1VRUN	VDDAN_11_CLK 1.1V 0.4A
+1_1VSUS	VDDRF_GBE_S
+3.VSUS	VDDIO_33_GBE_S 3.3V
+1_1VSUS	VDDCR_11_GBE_S 1.1V
+1_1VSUS	VDDIO_GBE_S 3.3V
+3VSUS	VDDIO_33_S 3.3V 0.049A
+1_1VSUS	VDDCR_11_S 1.1V 0.165A
+1_1VSUS	VDDCD_11_USB 1.1V 0.05A
AZ_VDDIO_DUAL	VDDIO_AZ_S 3.3V OR 1.5V 0.015A
+1_1VSUS	VDDCR_11_USB_S 1.1V
+3VRUN	VDDPL_33_SYS 3.3V SYS PLL 0.085A
+1.1VRUN	VDDPL_11_SYS 1.1V SYS PLL 0.06A
+3VSUS	VDDPL_33_USB_S 3.3V USB PLL 0.01A
+3VSUS	VDDAN_33_S 3.3V HWM 0.01A
+3VSUS	VDDXL_33_S 3.3V 0.005A

DDRIII SODIMM2--SYSTEM	
+1_5VDIMM	VDD MEM 4A
MEM_VTT	VTT_MEM 0.5A
LCD PANEL	
+3VRUN	3.3V 1.5A
PWR_SRC	5V 0.3A
USB 3.0	
+5VSUS	5VDual 0.9A
+3VSUS	VDD33 0.05A
+1.05VSUS_LDO	VDD11 0.6A
USB X2 FR	
+5VSUS	5VDual 0.5A*2
MINI PCIE SLOT0,1	
+1_5VRUN	1.5V (S0, S1) 0.5A each
+3VRUN	3.3V (S0, S1) 1.5A each
SATA HD0,1	
+5VRUN	3.3V (S0, S1) TBD
	5V (S0, S1) 0.9A
CPU FAN	
+5VRUN	5.0V (S0, S1) 0.5A
GIGA LAN	
+1_0V_SWITCH	1.0V CORE 0.3A
+3VSUS	3V ANALOG 0.16A
HD CODEC	
+5VRUN	5V CORE 0.3A
+3VRUN	3V ANALOG 0.1A
AUDIO OP	
CARDREADER	
+3VRUN	3V CORE 0.45A
+3.3V_CARD_SWITCH	3V_CARD 0.25A

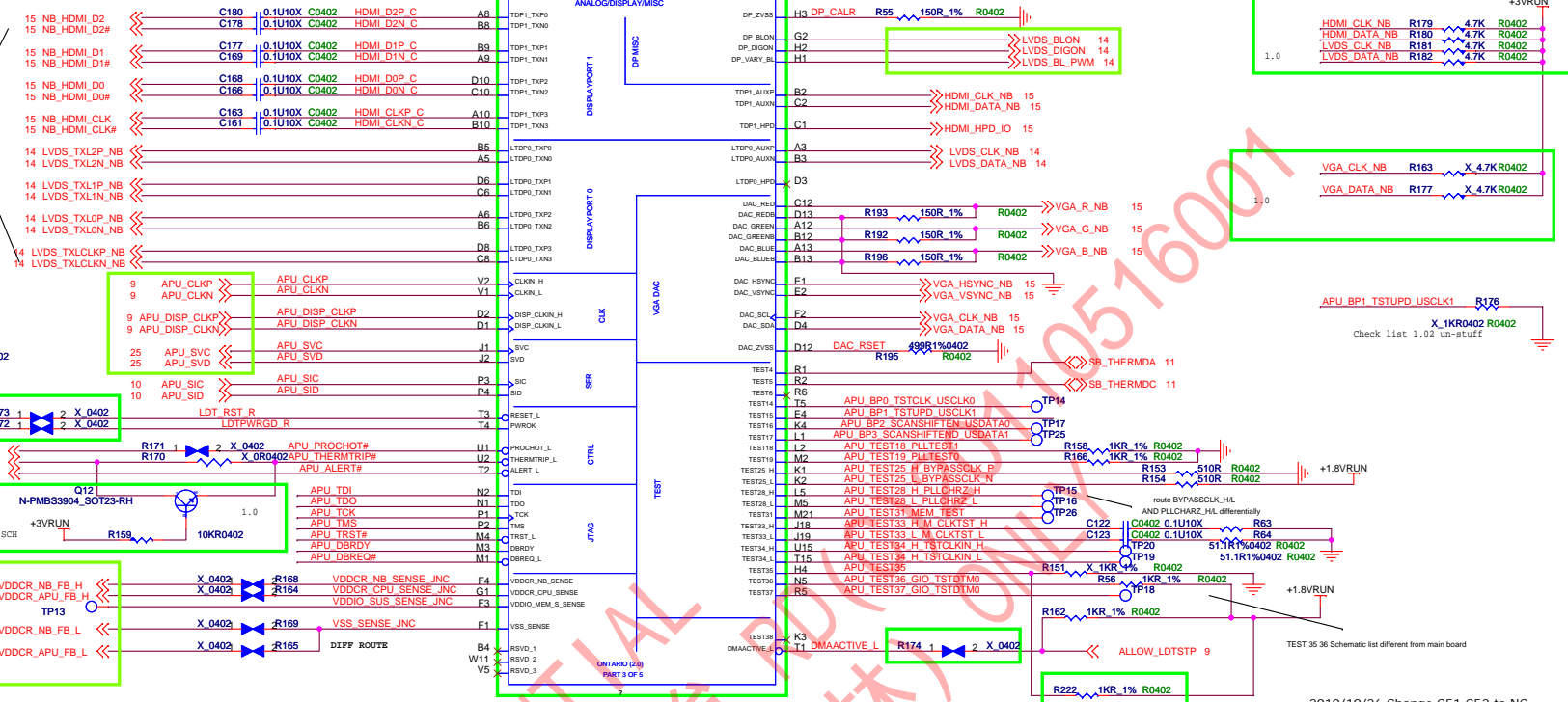


INTERNAL CLOCK MODE



CHECK FT1 Design
guides 45339 chapter
8;schematic checklist
45340

LVDS Check list 1.01 different
From design guides chapte 8



2010/10/26 Change U13 from
OA0-1245002 to OA0-1245004 for CPU
Ver. upgrade

2010/11/30 Change U13
from OA0-1245004 to OA0-16GN001
for AMD free sample

2011/01/04 Change U13 from
QA0-16GN001 to A10-K141605-A08

Debug R143 +1.8V

R139
R138

CPU_TCK	2	APU_TCK	1	KR0402	R0402
CPU_TMS	4	APU_TMS	1	KR0402	R0402
CPU_TDI	6	APU_TDI	1	KR0402	R0402

CPU_TDI	8	APU TDO 1KR0402 R0402
CPU_TDO	10	APU PWRGD# BUF
PWROK_BUF	12	LDT_RST# BUF

APU_DBRDY# R128

U_PLLTEST0	18	300R0402	R0402	APU
U_PLLTEST1	20	APU_TEST18_PLLTEST1		

11 to NC

ST TO NC

100%

Page 10 of 10

SY0402

R146 +1.8VRUN

RGD#_BUF

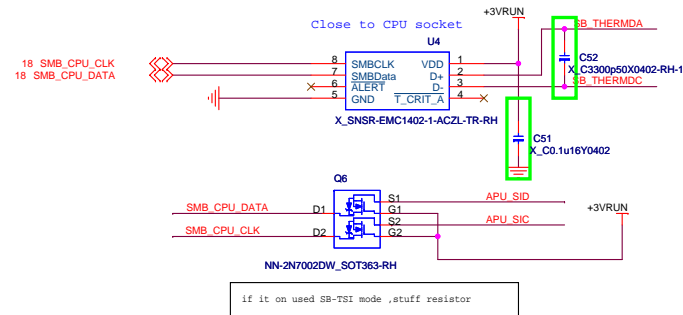
X_1KR0402 R0402

-6-RH

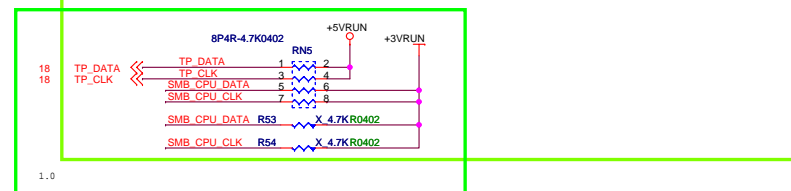
change U10,C229,R145,R146 to NC

3

2010/10/26 Change C51,C52 to NC

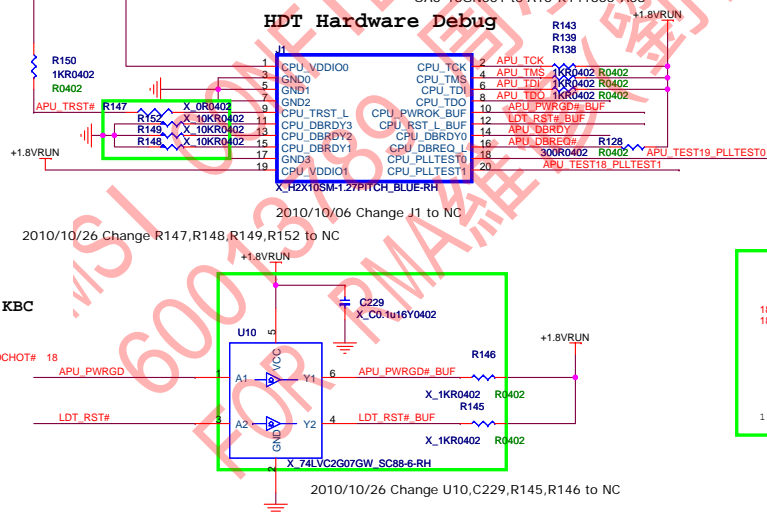


```
if it on used SB-TSI mode ,stuff resistor
```



HDT

HDT Hardware Debug

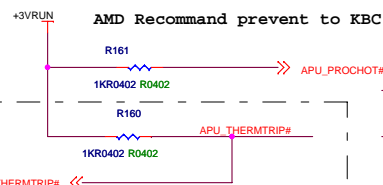


2010/10/26 Change R147,R148,R149,R152 to NC

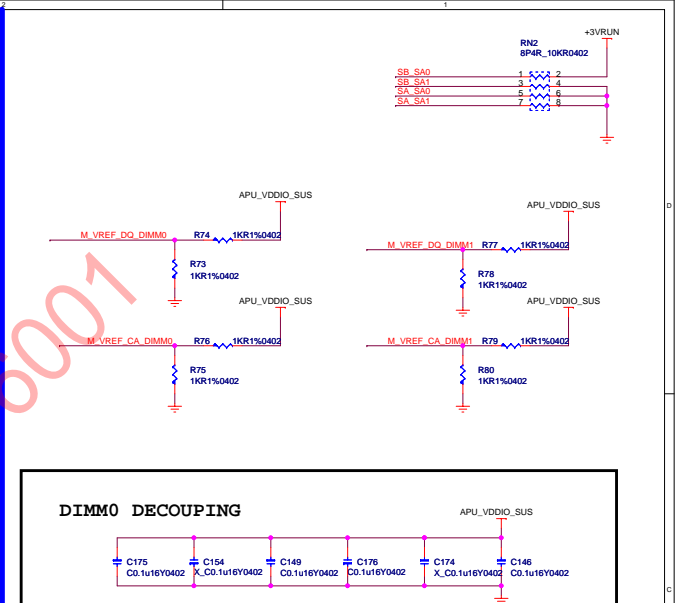
+1.8V RUN

2010/10/26 Change U10,C229,R145,R146 to NC

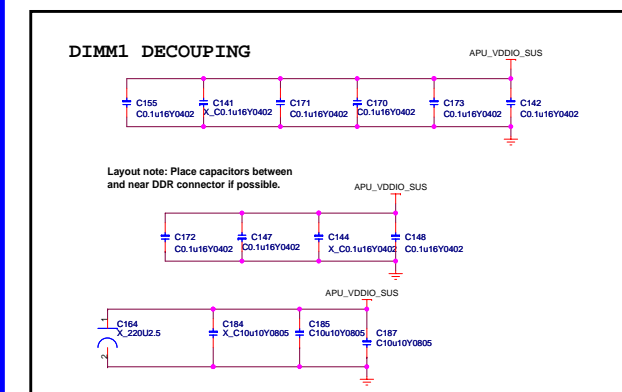
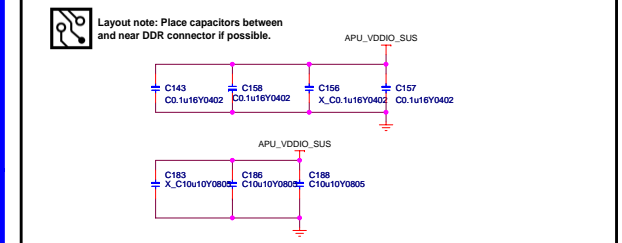
AMD Recommand prevent to KBC



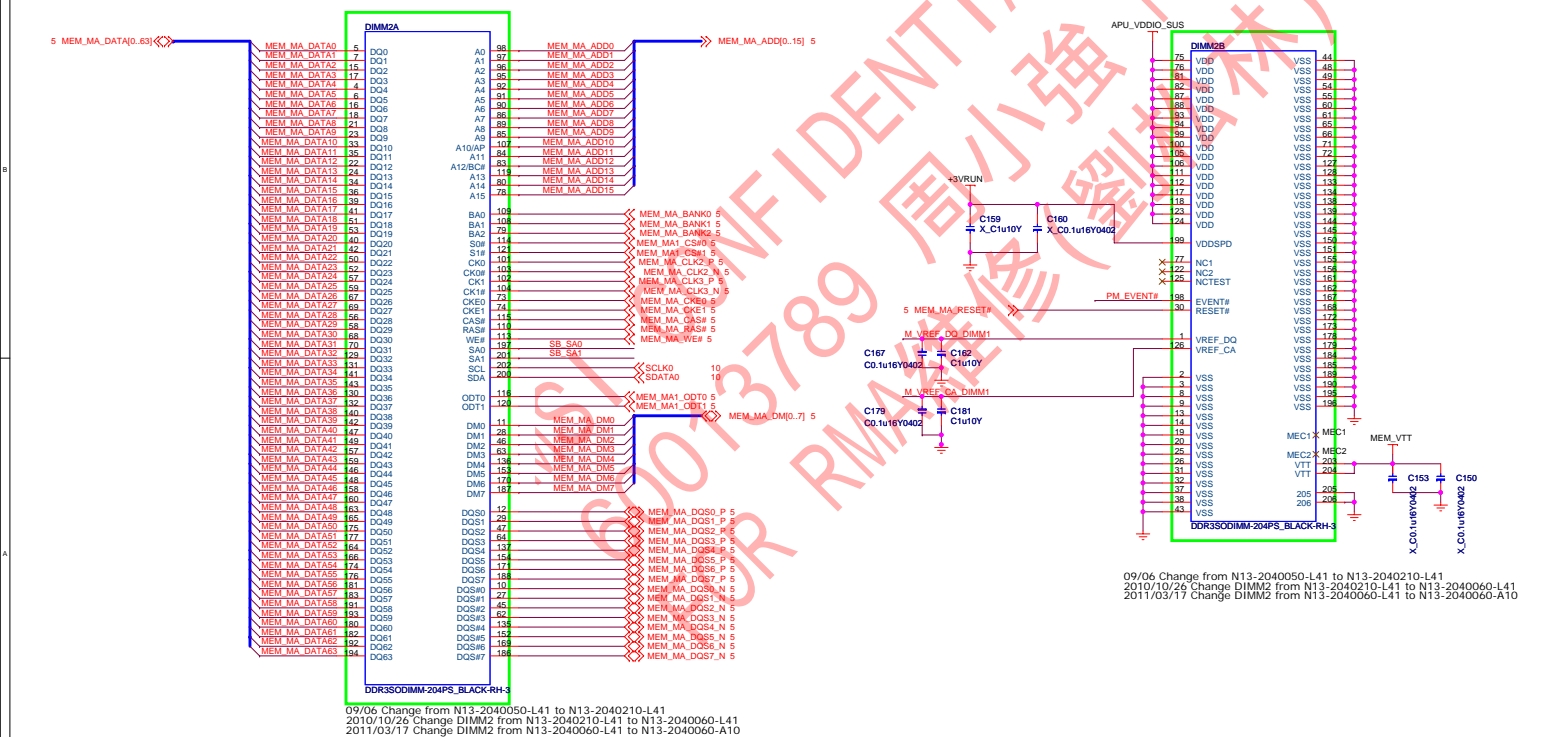
hudson-m1 Internal pull-up resistor to +3.3V-S5 is disabled to prevent leakage when APU is powered down.



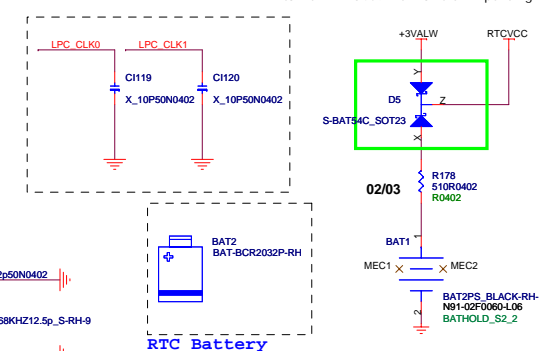
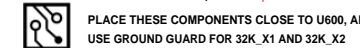
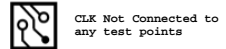
2011/03/17 Change DIMM1 from N13-2040050-L41 to N13-2040010-A10




09/06 Change from N13-2040050-L41 to N13-2040210-L41
2010/10/26 Change DIMM2 from N13-2040210-L41 to N13-2040060-L41
2011/03/17 Change DIMM2 from N13-2040060-L41 to N13-2040060-A10



09/06 Change from N13-2040050-L41 to N13-2040210-L41
2010/10/26 Change DIMM2 from N13-2040210-L41 to N13-2040060-L41
2011/03/17 Change DIMM2 from N13-2040060-L41 to N13-2040060-A10



 MICRO-STAR INT'L CO.,LTD.	
Title	
HUDSON PCIE/CLK/FCH	
Size	Document Number
Custom	MS-16GN1
Date:	Wednesday, May 04, 2011
Sheet	9 of 41
Rev	0.A

pcie wake pull-high page 20

internal pull-high

PLACE CLOSE TO SOUTH BRIDGE

schematic check
list 1.01:removed
support for the
integrated GBE MAC

HUDSON-M1 does not
support KBC function

the clock are not available in
the S5 domain
2010/10/26 Change R89 to Stuff for
RTS5139 use 48MHz solution

PLACE THESE PCIE RESISTOR CLOSE TO U600

usb any trace L1 <18"

USB [0:4]:[5:9] (10:13) BMCI
PORT:Disable BMCI Port have
optimization battery life

Bluetooth

Wireless

WebCamera (LVDS connector)

MiniPCIE1

CardReader RTS5139

USB 3.0_1 (BTB connector)

USB 2.0 (BTB connector)

USB 3.0_2 (BTB connector)

STRAP pin to define
use LPC or SPI ROM

HUDSON-M1 does not
support KBC function

FCH RESET



SATA trace should use only 1via on the trace. customers can use 2vias with GND via within 150mils of signal via as long as they can ensure that their platform meets SATA logo requirements. Return loss is expected to get affected with 2 vias. AMD platforms are validated with one via only

HDD

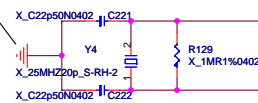
ODD

16	SATA_TX0P	C0.01u16X0402	C269	SATA_TX0P_C	AH9
16	SATA_TX0N	C0.01u16X0402	C270	SATA_TX0N_C	AJ9
16	SATA_RX0P	C0.01u16X0402	C271	SATA_RX0P_C	AJ8
16	SATA_RX0N	C0.01u16X0402	C272	SATA_RX0N_C	AH8
16	SATA_TX1P	C0.01u16X0402	C282	SATA_TX1P_C	AH10
16	SATA_TX1N	C0.01u16X0402	C280	SATA_TX1N_C	AJ10
16	SATA_RX1P	C0.01u16X0402	C281	SATA_RX1P_C	AG10
16	SATA_RX1N	C0.01u16X0402	C279	SATA_RX1N_C	AF10

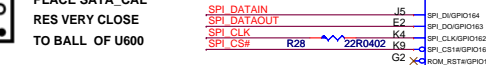
SATA PORTS DISTRIBUTION:
0, 2.5 INCH DISK DRIVER
1, SATA ODD
2, eSATA
3, 4 & 5, NOT USED



not used, data clock is generated internally using 25mhz reference clock



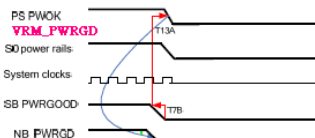
PLACE SATA_CAL RES VERY CLOSE TO BALL OF U600



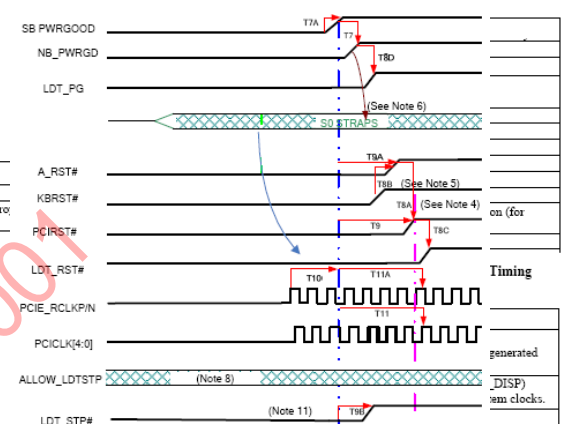
2010/10/26 Delect BIOS3 and change U7 from N14-0080030-L06 to M31-25F1602-E17 for remove BIOS socket



2011/03/24 Add LAB1



	Min.	Max.	Description
T7B	-	1 ms	SB PWR_GOOD fail time.
T13A	80 ns	-	SB PWR_GOOD must be de-asserted before VDD (PS PWOK) drop more than 5% off the nominal value. See Note 9.



Symbol	Min.	Max.	Description
T7	-	-	[Not illustrated] SB PWRGOOD to clock out (clocks are not stable at this point)
T7A	-	50 ms	See Table 33 and Table 34 below.
T8A	0 ns	100 ms	A_RST# (PCI host bus reset) to PCIRST#.
T8B	-	Note 5	KBRST# to A_RST#.
T8C	1.0 ms	2.3 ms	PCIRST# to LDT_RST#.
T8D	77 ms	108 ms	NB_PWRGD to LDT_PG.
T9	101 ms	113 ms	SB PWR_GOOD to PCIRST#.
T9A	101 ms	113 ms	SB PWR_GOOD to A_RST# (T9-T8A).
T9B	31 ms	-	SB PWR_GOOD to LDT_STP#.
T10	-31 ms	-	PCIE_CLKP/N stable time before SB PWRGOOD assertion (for external clock mode only).
T11	36 ms	41 ms	SB PWR_GOOD to stable PCIECLK 33 MHz. See Note 8.

Table 33. Power Sequence SB PWRGOOD, NB_PWRGOOD, and System Clock Timing (For Internal Clock Mode Only)

Symbol	Min.	Max.	Description
T7	40ms	42ms	SB PWRGOOD assertion to NB_PWRGD assertion delay. Note: This timing only applies to the NB_PWRGD signal generated from SB820M.
T11A	-	38 ms	SB PWRGOOD to stable system clocks (CPU, PCI-E, NB_DISP) when SB820M clock function is enabled to provide all system clocks.
T11B	-	32 ms	[Not illustrated] SB PWRGOOD to clock out (clocks are not stable at this point).
T8D	58 ms	108 ms	NB_PWRGD to LDT_PG.

Table 34. Power Sequence SB PWRGOOD, NB_PWRGD, and System Clock Timing (For External Clock Mode Only)

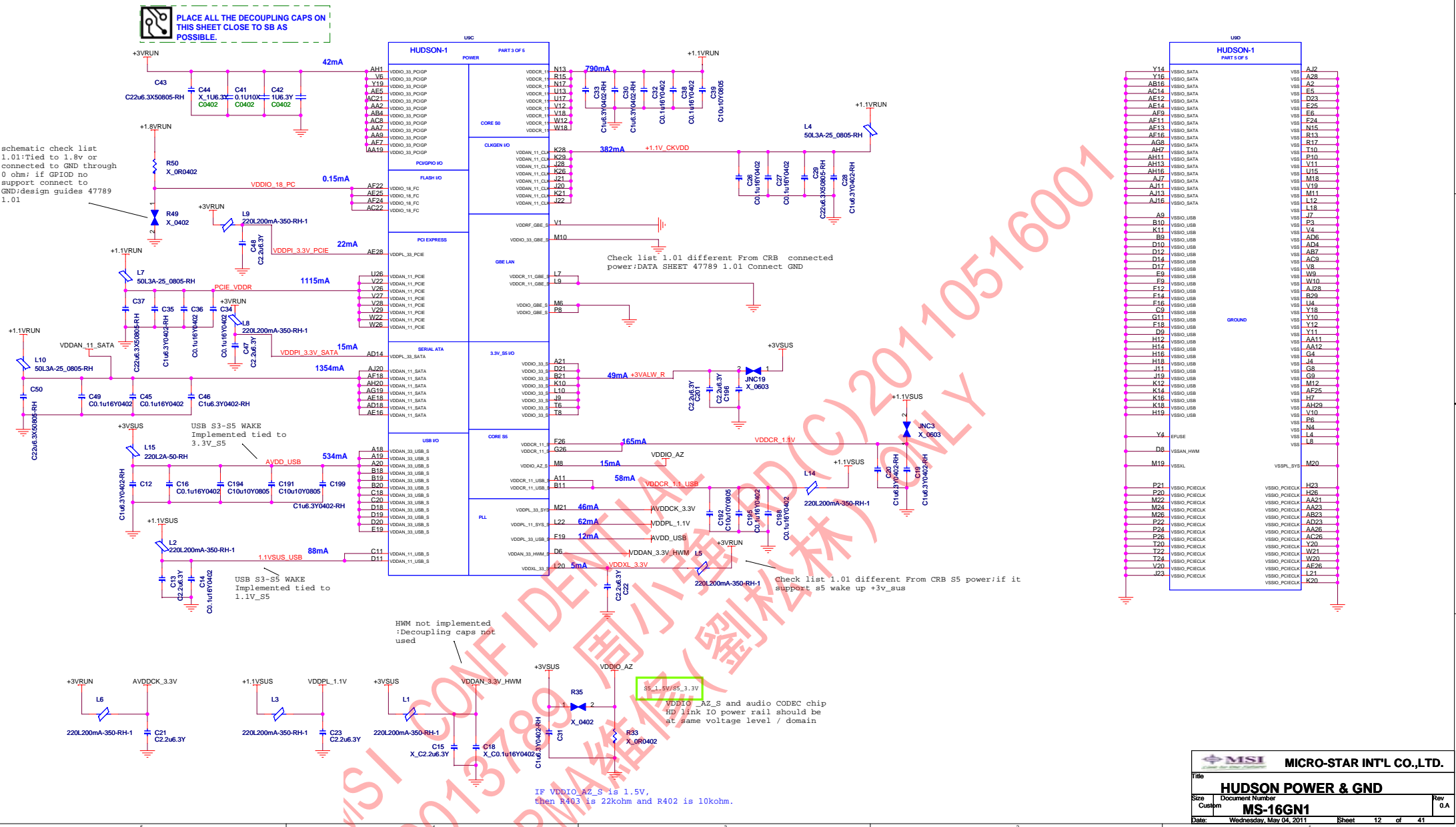
Symbol	Min.	Max.	Description
T7	0ns	30ns	SB PWRGOOD assertion to NB_PWRGD assertion delay when using the SB820M NB_PWRGD output.

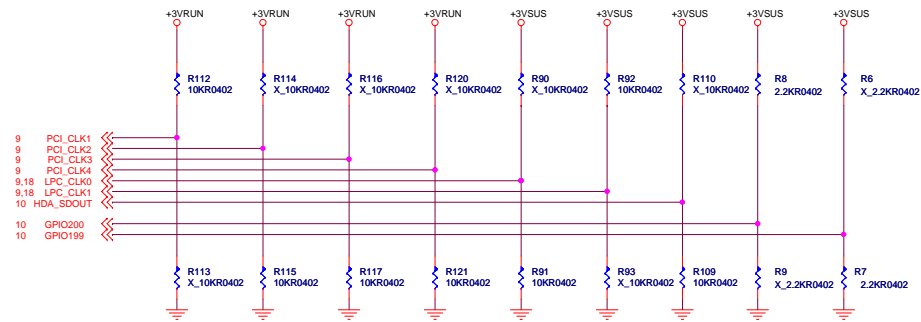
Note 4: Typical time between A_RST# and PCIRST# is 75 ns. The measurement should be done at 10% of both signals. Loading on the motherboard may cause the measurement at 90% be more than the spec.

Note 5: The KBRST# should be de-asserted before A_RST# (LDT_RST#) is de-asserted.

Note 6: Type II Standard and Debug straps will be latched after SB PWR_GOOD is asserted. Type I straps are latched on resume reset rising edge.

Note 8: The PCI Clock may be stable before T11 min. under some conditions; however in all cases, the PCI Clock is guaranteed to be stable only between T11 min. and max.

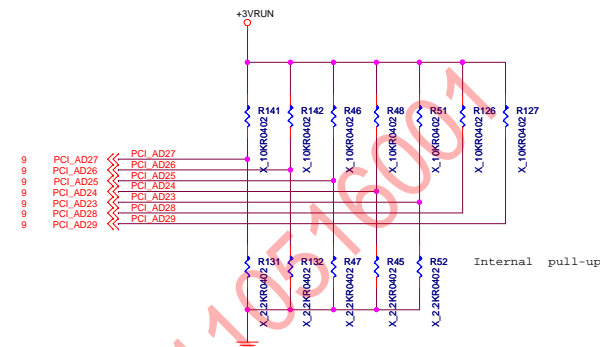




REQUIRED STRAPS

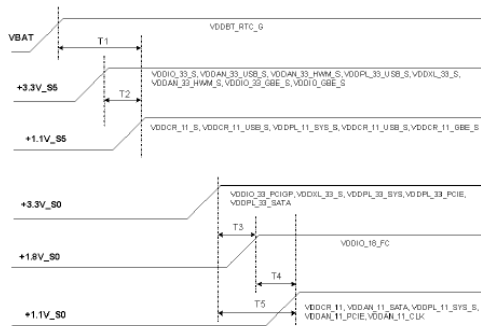
PCI_CLK4: Applicable to internal clock gen mode only check list 1.01

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H.H = Reserved H.L = SPI ROM (Default)	
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED	CLKGEN DISABLED	L.H = LPC ROM L.L = FW ROM	



DEBUG STRAPS

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



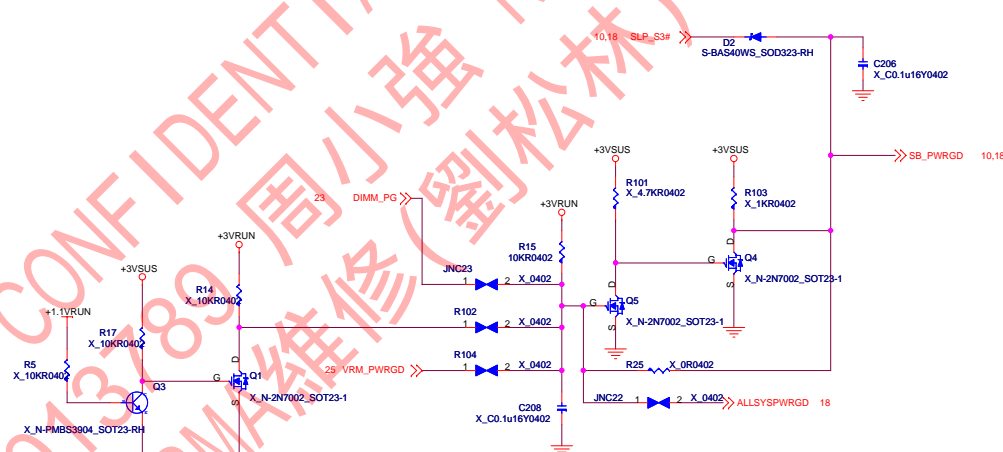
Symbol	Parameter	Voltage Difference During Ramping	
		Minimum (V)	Maximum (V)
T1	VBAT ramps high relative to the S5 rails.	See Note 1	No restrictions
T2	+3.3V_S5 rails ramp high relative to +1.1V_S5 rails.	0	No restrictions
T3	+3.3V_S0 rails ramp high relative to +1.8V_S0 rails.	0	No restrictions
T4	+1.8V_S0 rail ramps high relative to +1.1V_S0 rails.	0	No restrictions
T5	+3.3V_S0 rails ramp high relative to +1.1V_S0 rails.	0	No restrictions

Note 1: VBAT (VDDBT_RTC_G) must ramp at least 5 seconds before the S5 rails to allow start time for the internal RTC.

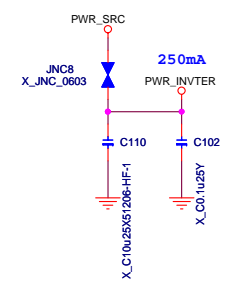
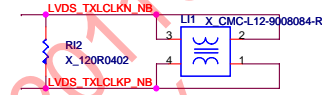
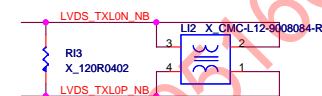
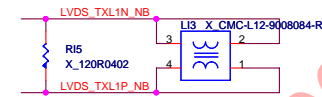
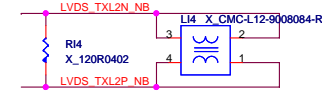
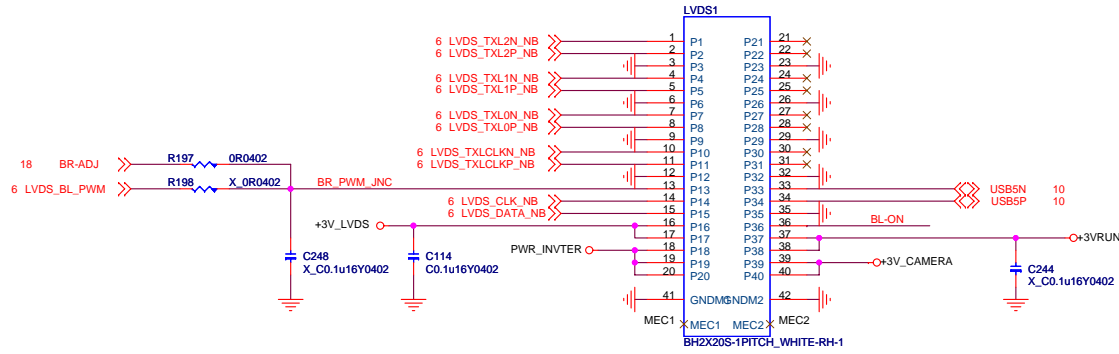
Note 2: For power down, the rails should either be turned off simultaneously or in the reverse of the order shown above. Variations in speeds of decay due to different capacitor discharge rates can be safely ignored. The VDDIO_33_S (S5_3.3V) power-rail ramp-down time must be more than 300 μ s.

Note 3: Power rails from the same group are assumed to be generated from the same regulator. However, they can be generated from different regulators if all other requirements are met.

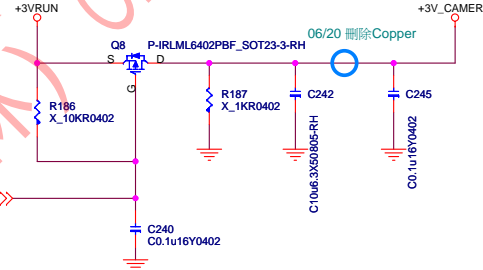
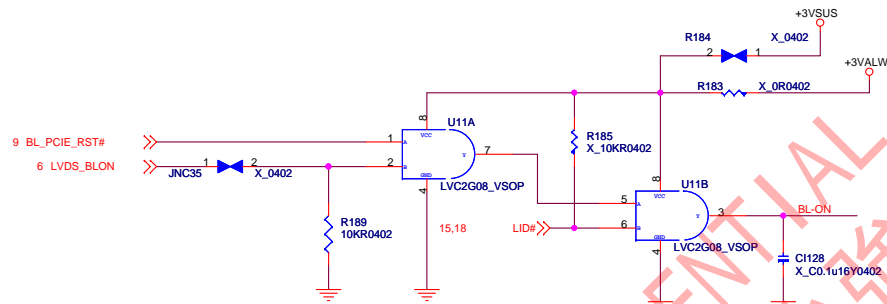
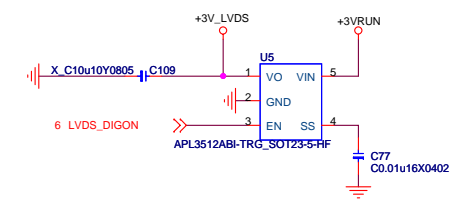
Note 4: The ramp-up time for all power rails except VDDIO_33_S must be in the 50 μ s to 40 ms range (50 μ s \leq All power rails except VDDIO_33_S \leq 40 ms). However, the ramp-up time for VDDIO_33_S must be in the 100 μ s to 40 ms range (100 μ s \leq VDDIO_33_S \leq 40 ms).



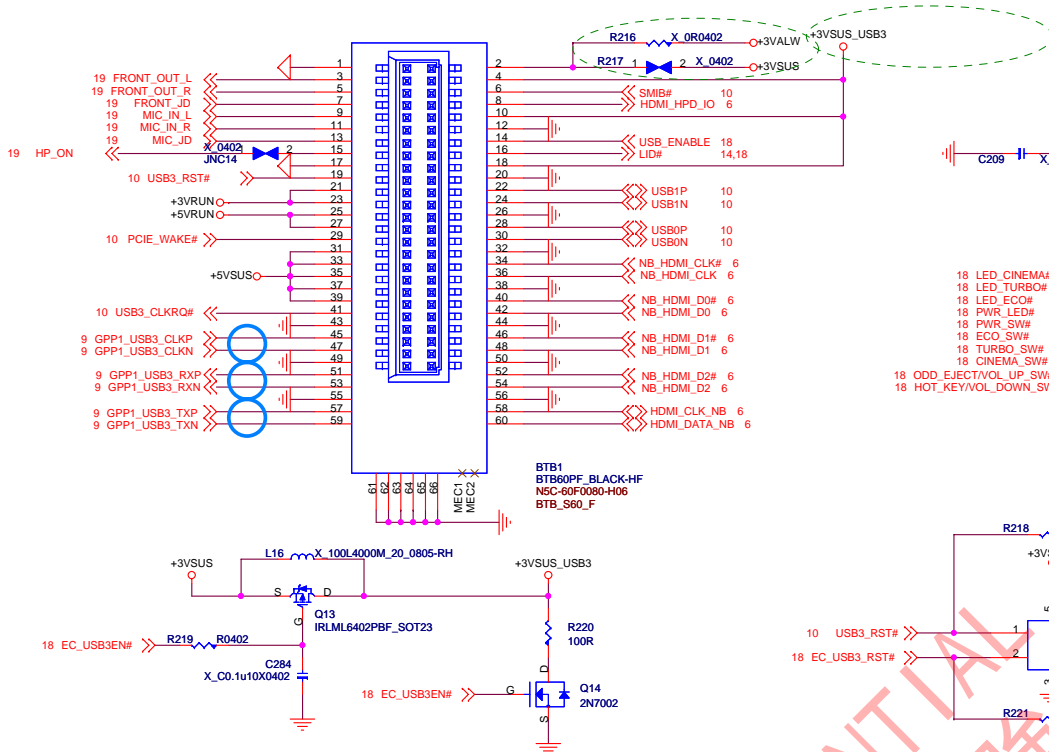
LVDS



LVDS POWER

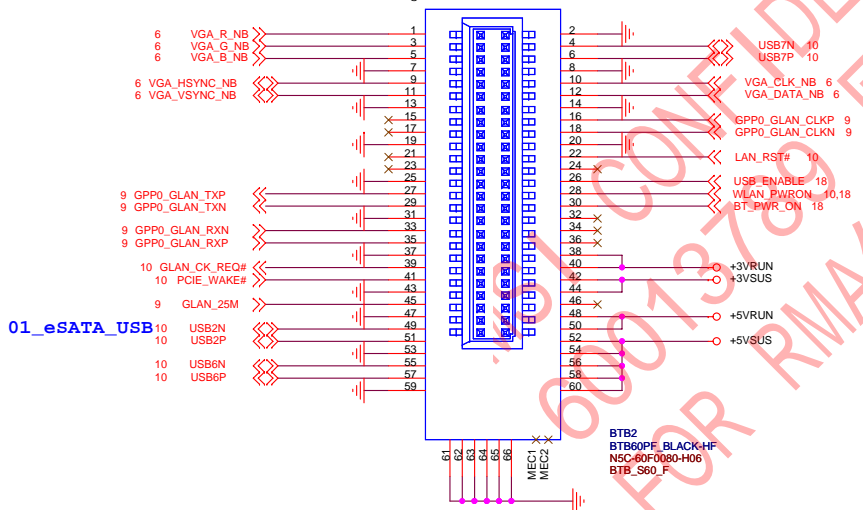


(16GNB) - HDMI/Audio/USB3.0

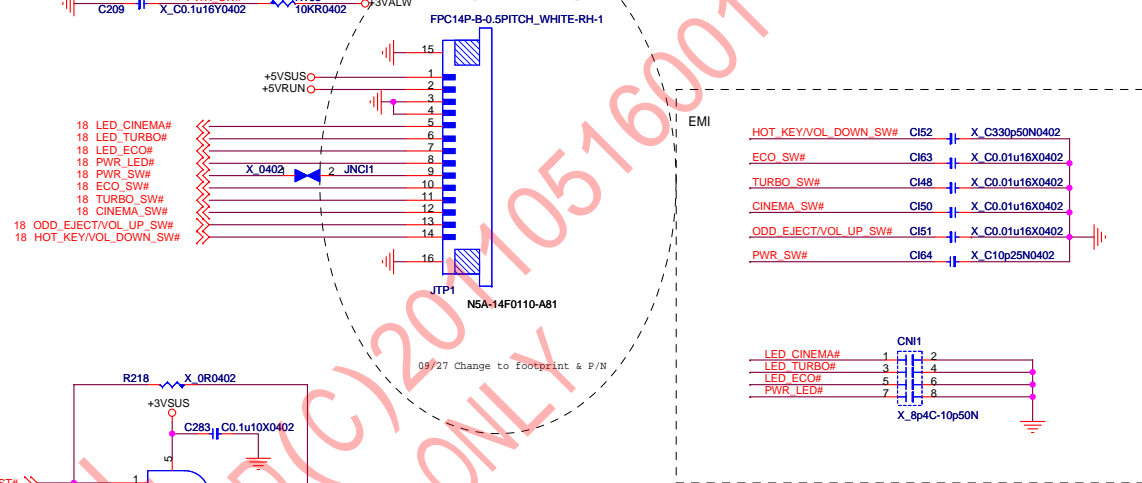


(16GNA) - CRT/USB2.0/GLAN

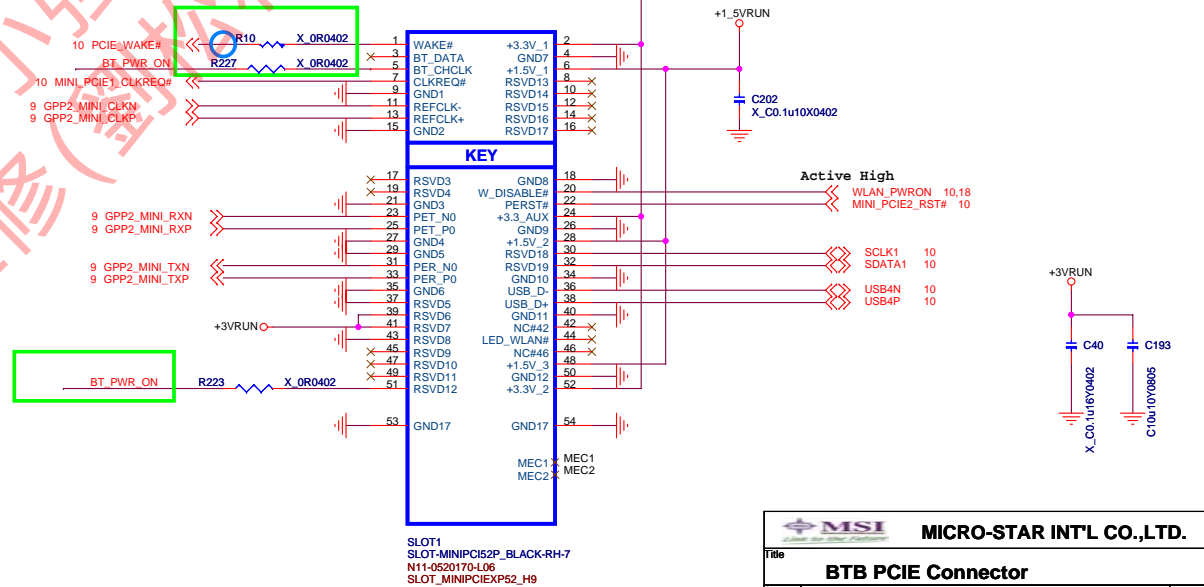
2011/02/23 Change Q14 from D03-0700249-P03 to D03-0700299-F09 for costdown



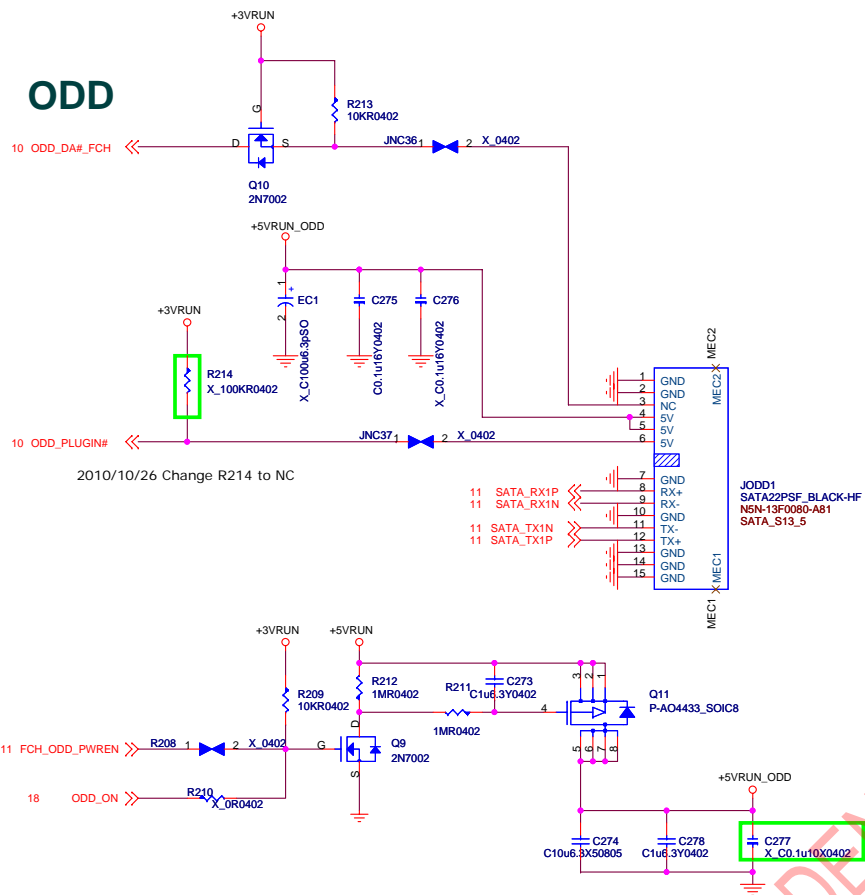
(16GNC) - Power Board



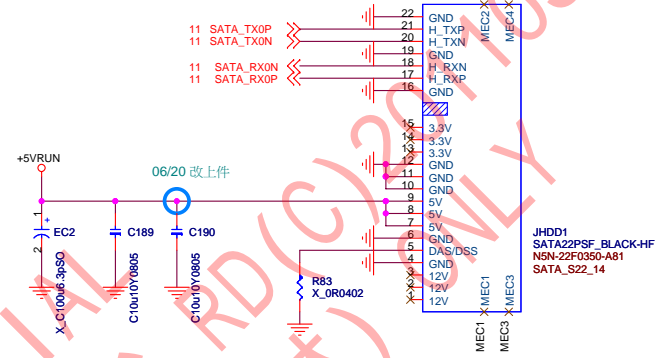
WLAN



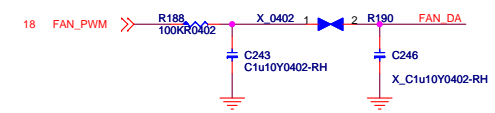
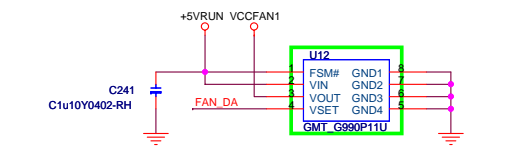
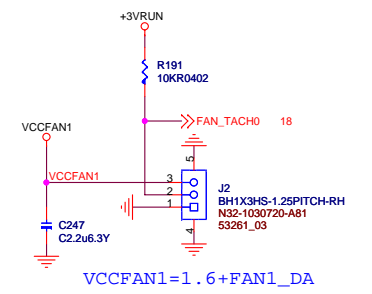
ODD

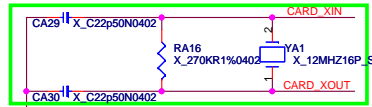


HDD

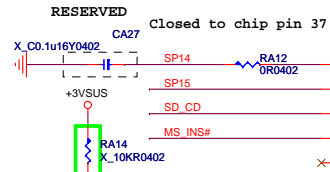


FAN





2010/10/26 Change YA1, RA16, CA29, CA30, RA14 to NC for RTS5139 use 48Mhz solution



+3VSUS

RA18

X_100KR0402

10 CLK_48M_USB

JNC161

2 X_0402

CARD_XIN

CARD_XOUT

XTLCLK_IN

XTLO

RST#

NC

DV18

RREF

CA34

100p50

C0402

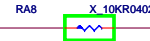
2011/01/11 Change CA31 from C11-1053312-W08 to C11-1011032-W08 and stuff for fix RTS5139 disappear issue

Clock	MODE1	MODE0
48MHz	X	X
24MHz	X	O
12MHz	O	X
12MHz (Crystal)	O	O

10 USB3N
10 USB3P

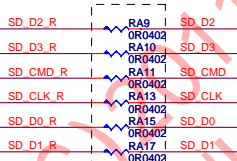
DM DP NC NC NC NC NC NC NC NC 3V3 IN Card_3V3

2010/10/26 Change RA8 to NC for RTS5139 use 48Mhz solution



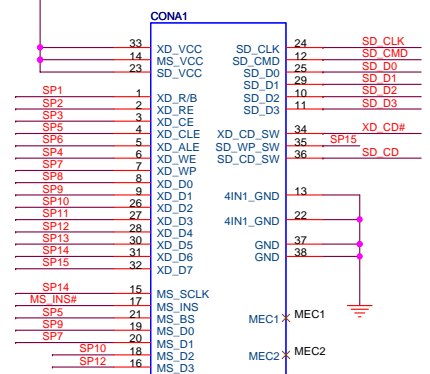
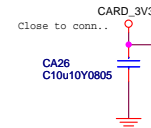
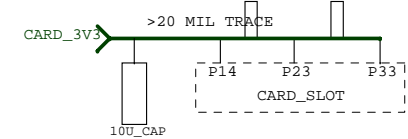
Closed to chip

RESERVED

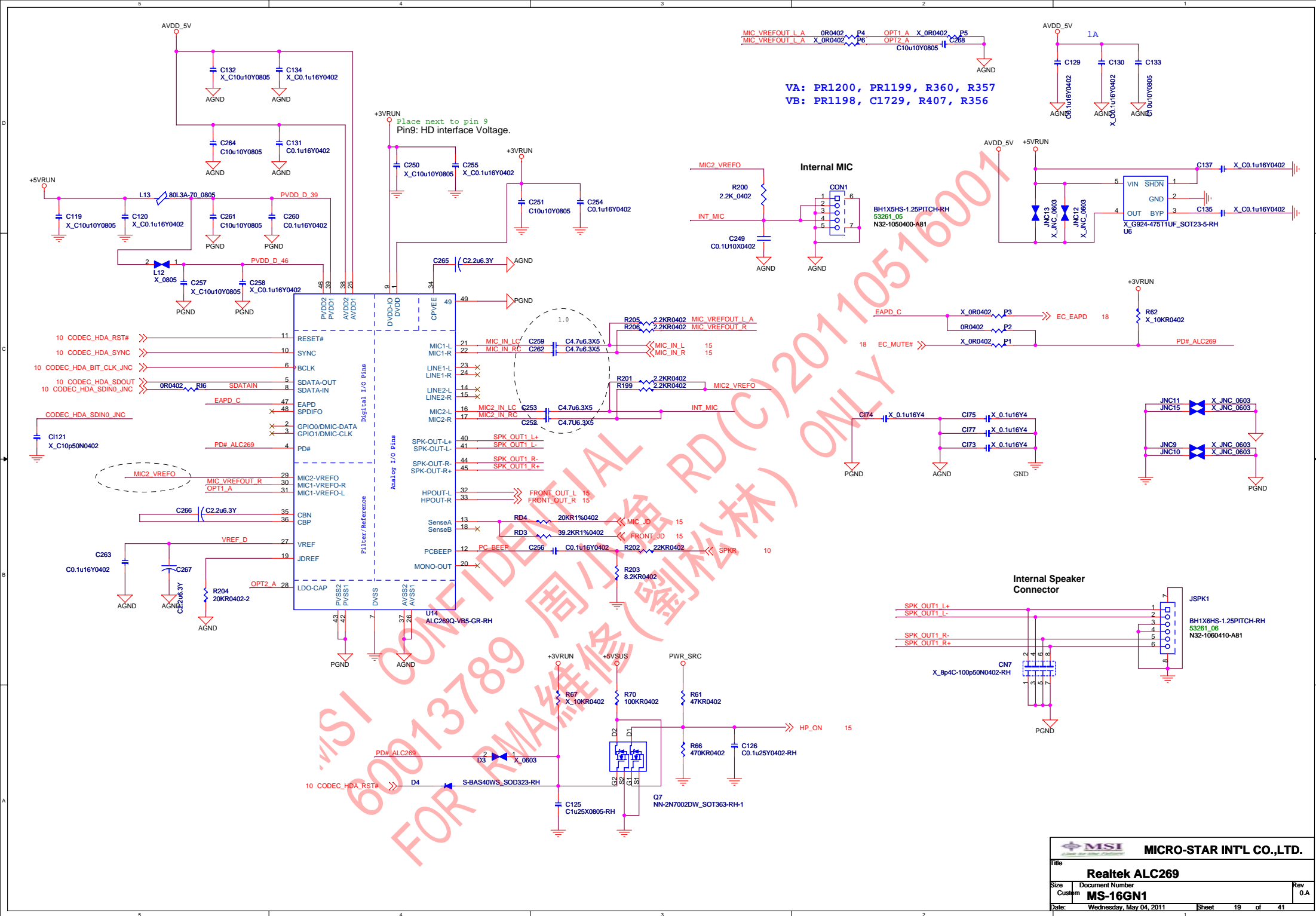


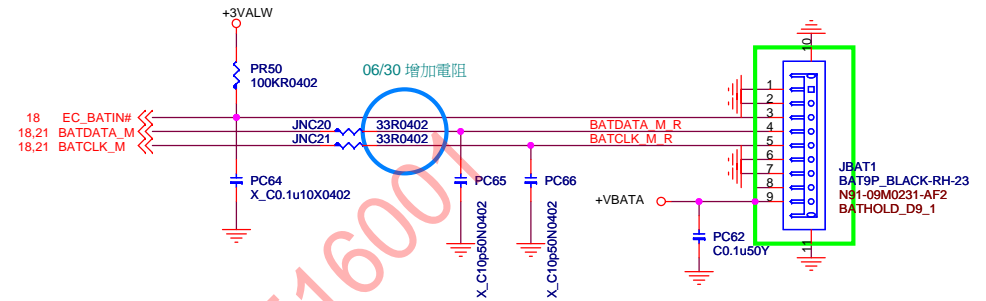
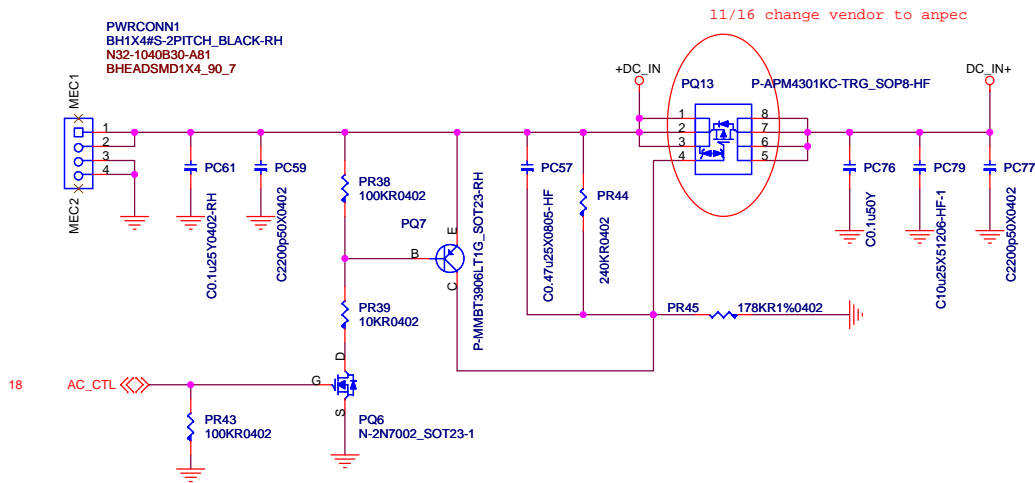
RESERVED

RESERVED



SD_MS MMC XD-RH-1
N56-38F020-TB4
IOASM_4IN1_38_1

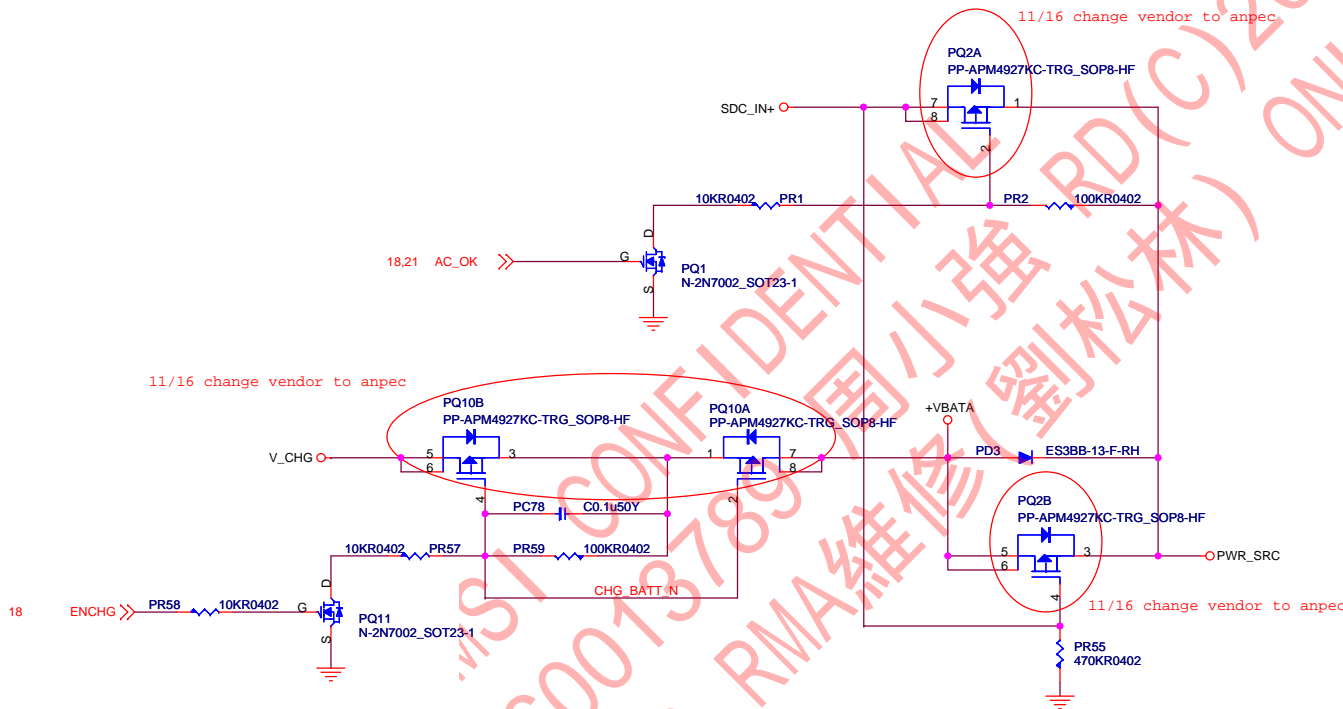




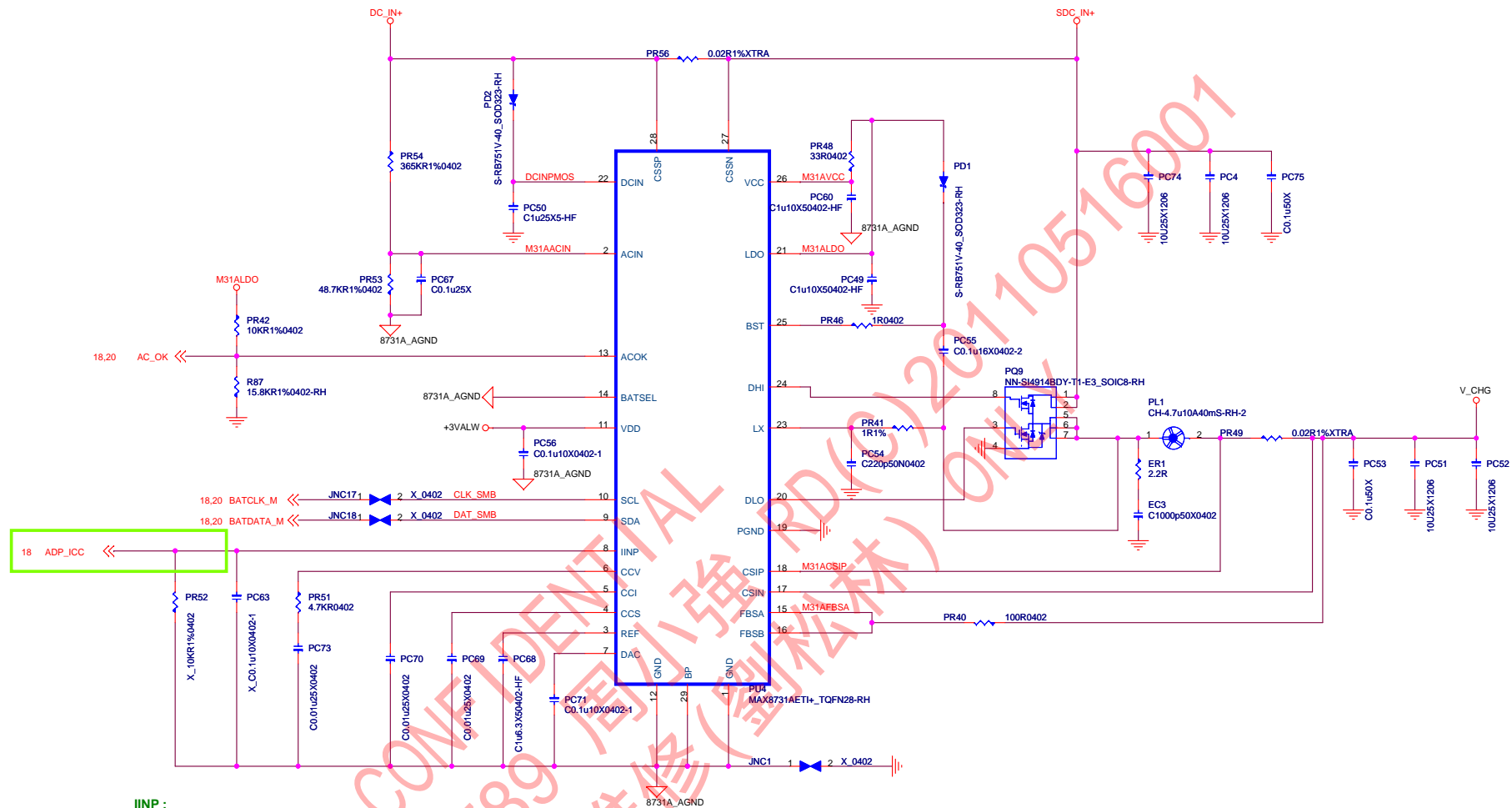
2010/10/06 Change JBAT1 from N91-09M0041-AF2 to N91-09M0231-AF2

JBAT1 Pin Definition

- 1: GND
- 2: GND
- 3: BAT_IN#
- 4: SMBDATA
- 5: SMBCLK
- 6: NC
- 7: NC
- 8: VBATA+
- 9: VBATA+



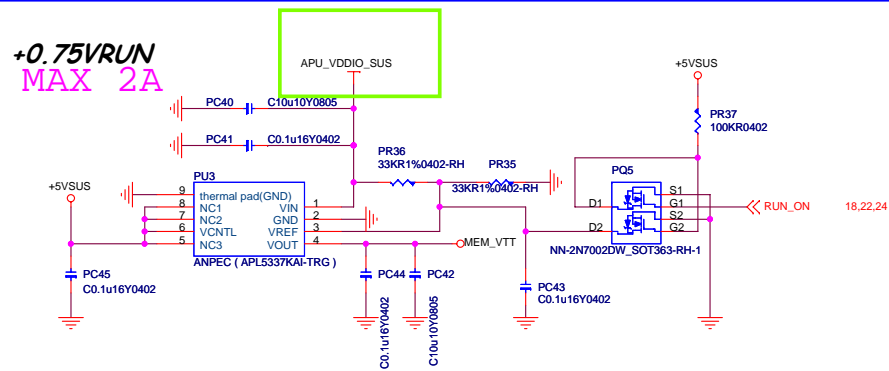
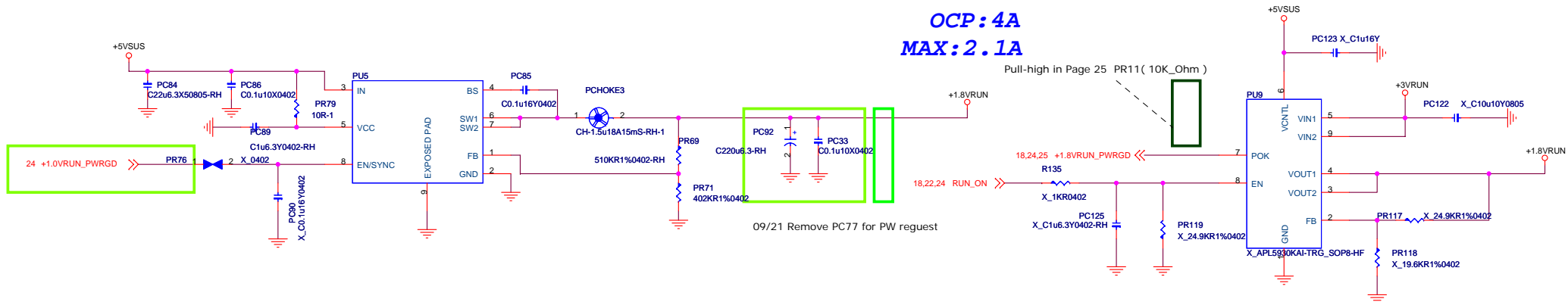
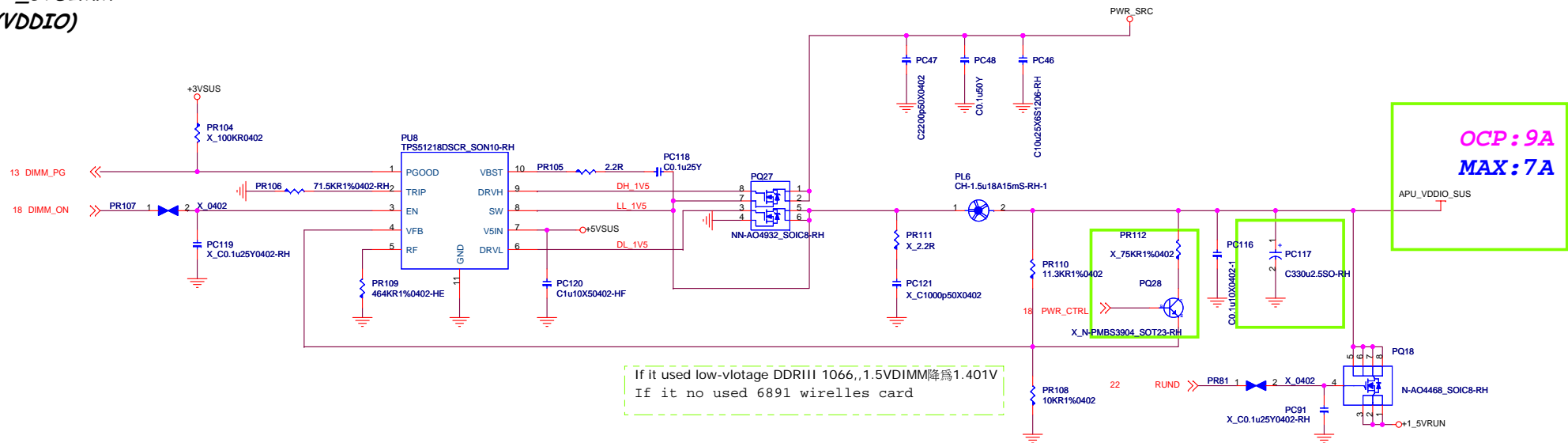
MSI MICRO-STAR INT'L CO.,LTD.			
Title			
Battery Select			
Size	Document Number		Rev
Custom	MS-16GM		1.0
Date:	Wednesday, May 04, 2011	Sheet	20 of 41

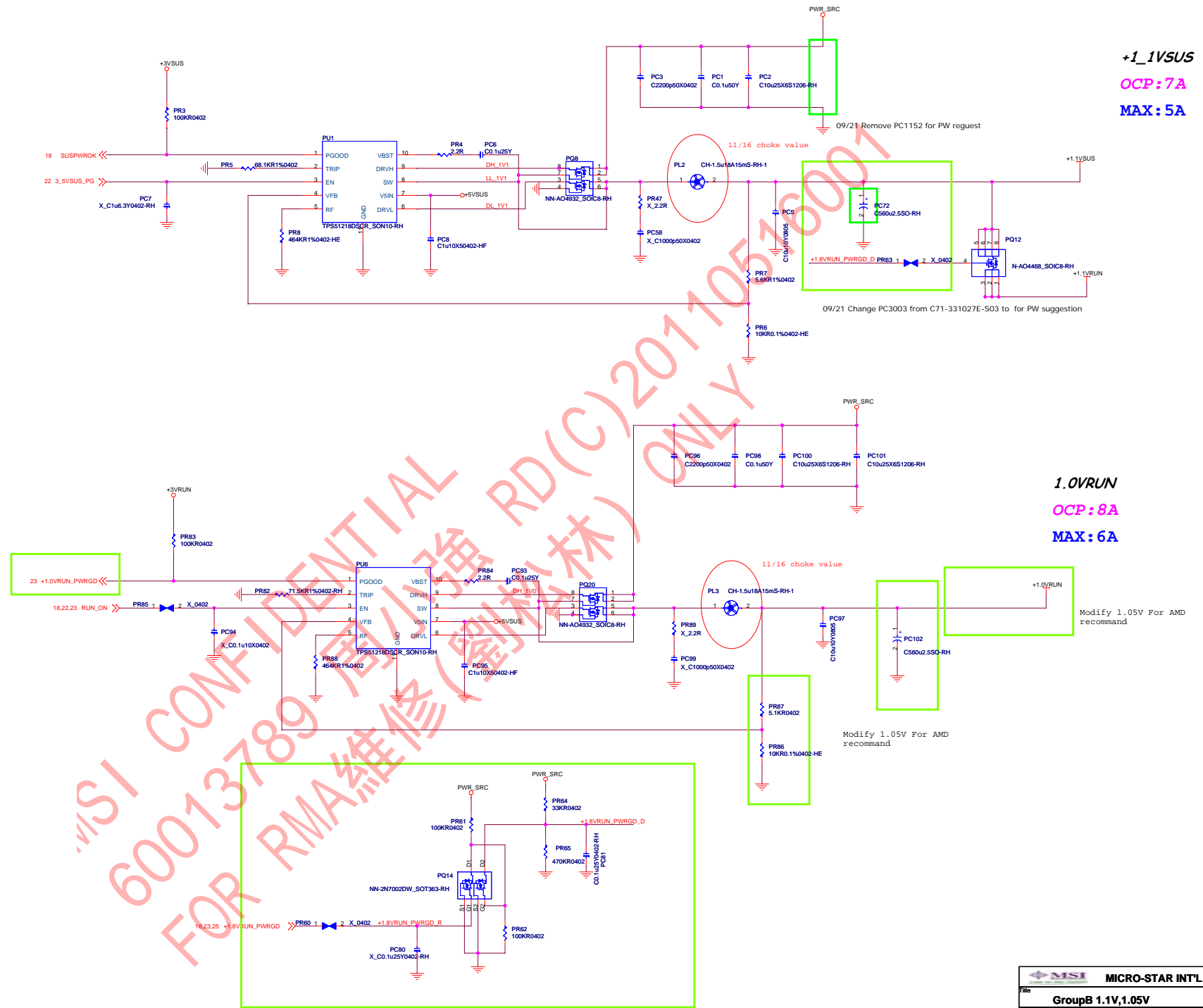


IINP :

1. The transconductance from (CSSP - CSSN) to IINP is 3mA/V.
2. $V_{IINP} = IINP \times RS1 \times 3mA/V \times PR25$

**+1_5VDIMM
(VDDIO)**





+1.1VSUS
OCp: 7A
MAX: 5A

1.0VRUN
OCp: 8A
MAX: 6A

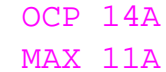
Modify 1.05V For AMD
recommand

Modify 1.05V For AMD
recommand

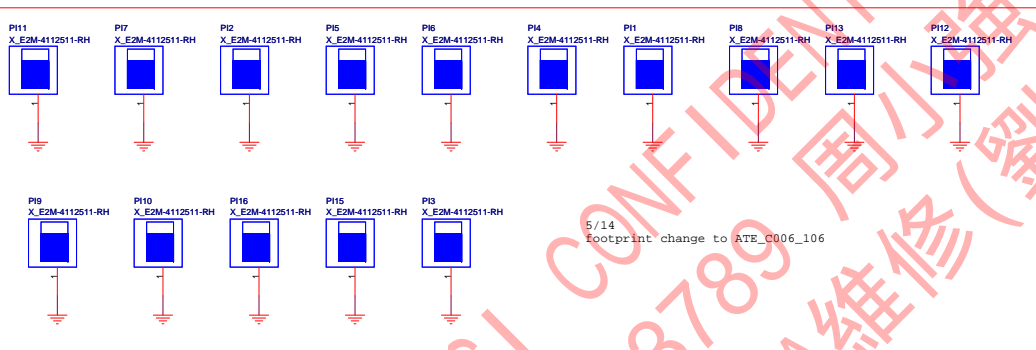
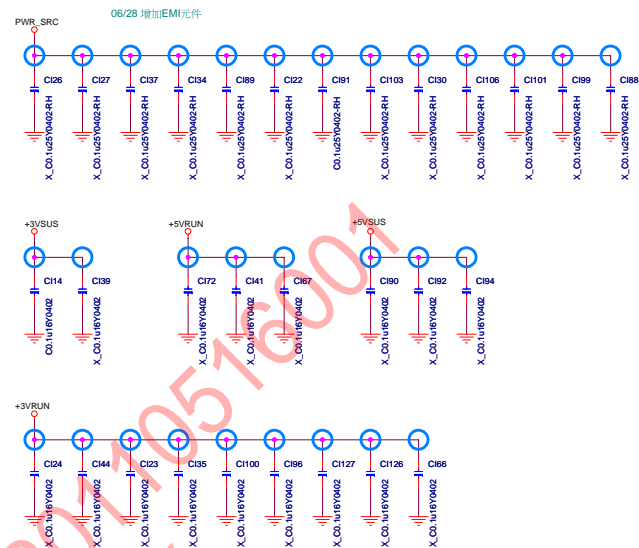
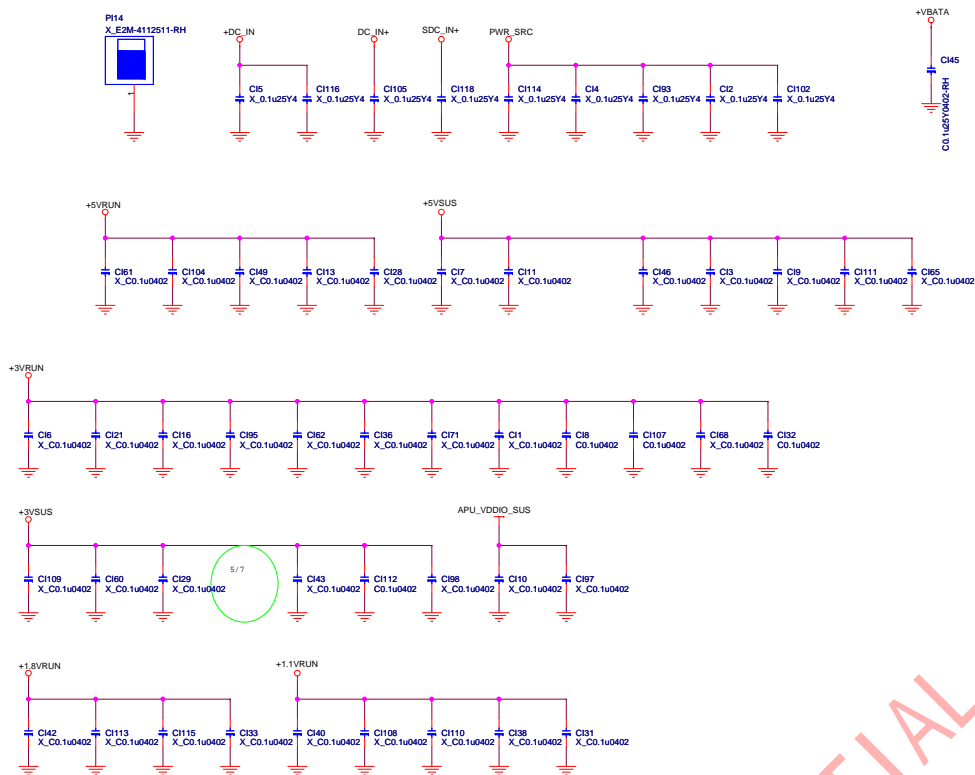
OFS/VFIXEN	Offset & Droop	SVI	VFIX
GND	O	O	X
+3.3V	X	X	O
+5V	X	O	X

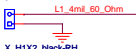



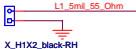

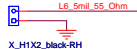
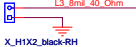

SVC	SVD	Output
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8



OCP 12A
MAX 10A



J14 	J20 	J37 	J18 	60 OHM
J4 	J13 	J5 		55 OHM
J38 	J39 			40 OHM

J6 	J9 	J3 	J28 	DIFF_100 OHM
J8 	J12 	J7 	J34 	
J17 	J16 	J33 	J25 	DIFF_90 OHM
J19 	J15 	J27 	J31 	
J10 	J29 	J38 		DIFF_85 OHM
J11 	J35 	J30 		
	J24 	J22 	J32 	DIFF_72 OHM
	J23 	J21 	J26 	

CPU Thermal Hole

CPU Thermal Model ASM CFG = 60

PCB

for HDMI Logo charge

NB STANDOFF

APU STANDOFF

2010/10/27 Change GPU_H1 and NB_H1 from E2B-1221010-L63 to E2B-16GM010-A89 for Thermal request

FCH STANDOFF

FCH Thermal Model ASM CFG = 60

Mylar for SAFETY

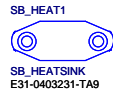
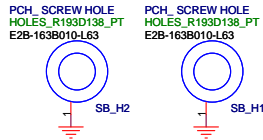
Mylar for M/E



Mylar for EMI



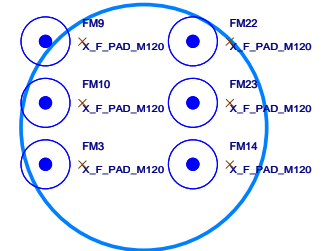
2010/01/18 Add RUBBER_5 for ME request
2011/03/15 Remove MYLAR_9,MYLAR_10,MYLAR_14 for costdown
2011/04/19 Change RUBBER_1,RUBBER_2,RUBBER_4 to NC for costdown



BTB3 SCREW HOLE (16GKA)

BTB1 STANDOFF (16GKB)

PCIE STANDOFF (Mini PCIE Card)



8/06 增加板邊光學測試點7顆

NPTH (only hole)

HDD Connector SCREW ASM CFG = 60

HDD Connector SCREW ASM CFG = 60



2010/01/10 Change Screw_ODD1,Screw_ODD2 from E43-1204005-H29 to E43-1205014-G68 for ME request